PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

Do not enter 9/19/2005

1. (Original) Apparatus to consolidate the output of data, the data comprising a plurality of data elements, the apparatus comprising:

a plurality of processors, each processor comprising:

an input register configured to receive a predetermined quantity of data elements;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the processed data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer a first portion of processed data elements to the appropriate butterfly processor to perform additional mathematical operations and, where if disabled, is configured to transfer a second portion of processed data elements to at least one holding register;

wherein the holding register is configured to store the processed data until all of the first portion data elements is processed; and

a plurality of output registers associated with the plurality of processors, wherein each output register is coupled to the holding register and another output register, each output register configured to receive the processed data from the holding register and route the processed data to an output register of a different processor.

2. (Original) The apparatus set forth in Claim 1, further comprising at least one input multiplexer coupling the feedback loop and the intermediate register, wherein each input multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate butterfly processor.

3. (Original) The apparatus set forth in Claim 1, further comprising at least one output multiplexer coupling the butterfly processor and the intermediate register, wherein each